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14. ABSTRACT
The feasibility of utilizing the GaN/AlGaN material system in the development of high power amplifiers for X-band frequencies and above was investigated. The GaN based heterojunction field effect transistor (HFET) on SiC shows remarkable power density at microwave frequencies. An order of magnitude improvement can be attained in output power when compared with present GaAs devices, judging from the already observed power density along with further anticipated advances of these GaN devices. Four individual HFET devices operating in combination were able to achieve 6 watts (W) output at 9.4 Ghz. The investigation into improving this performance for Phase II research is documented.

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Development of GaN Based Microwave Power Amplifier for X-Band Applications

SBIR Phase 1 Final Technical Report

Dr. Kevin W. Alt, Principal Investigator
Dr. Kang L. Wang, Scientific Consultant

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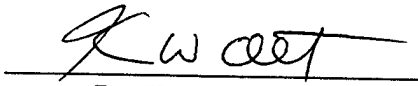
The Contractor, ProComm Enterprises, Inc., hereby declares that, to the best of its knowledge and belief, the technical data delivered herewith under Contract No. DASG60-99-M-0090, from 99MAY12 to 99NOV12, is complete, accurate, and complies with all requirements of the contract.



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SBIR Phase I Final Technical Report

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During Phase I of this research we have investigated the feasibility of utilizing the GaN/AlGaN material system in the development of high power amplifiers for X-band frequencies and above. GaN is a wide band gap material with high thermal conductivity, which can be directly grown on SiC or sapphire[1]. The GaN based heterojunction field effect transistor (HFET) on SiC shows remarkable power density at microwave frequencies. An order of magnitude improvement can be attained in output power when compared with present GaAs devices, judging from the already observed power density along with further anticipated advances of these GaN devices. With the high current, high voltage characteristics of the GaN devices, power amplifier circuits need to be designed differently. During Phase I of this study, we investigated the gain and output power achievable from these devices with differing device compositions and material makeup. Our feasibility study has shown that four individual HFET devices, as described below and referred to as a power amplifier when operating in combination are able to achieve 6 watts (W) output at 9.4 Ghz. Although this result falls somewhat short of our established goal of 20 W at the inception of this research, we project that power levels meeting and even exceeding this level will be achieved in the near future from a similar combination of four devices, given improved circuit design and devices.

I. *Abstract*

During this study, work was conducted on two basic levels. Before proceeding, we should clarify the difference between individual devices, power coupled devices, and

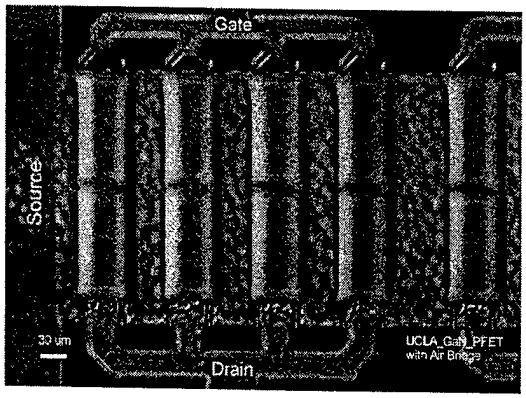


Figure 1. Parallel Finger Arrangement Utilized in HFET Device Structures

power amplifier packages. Fig. 1 shows an on wafer image of a power transistor assembly. In order to improve the current handling capability of the device while

managing the input impedance seen at the gate, it is fairly standard practice to process devices with multiple active regions connected in parallel. Thus, as seen in the image, there are actually eight gate electrodes running vertically through the structure. The source electrode seen at the far left of the image is connected to the common source regions utilizing an air bridge over the gate and drain regions to prevent short circuits while also providing a conduit for additional air cooling and heat removal. Each air bridge encompasses two gate electrodes and two active transistor regions. Fig. 2 illustrates two such bridges encompassing four active regions. A complete structure with four air bridges and eight active transistor regions will be referred to as a single device

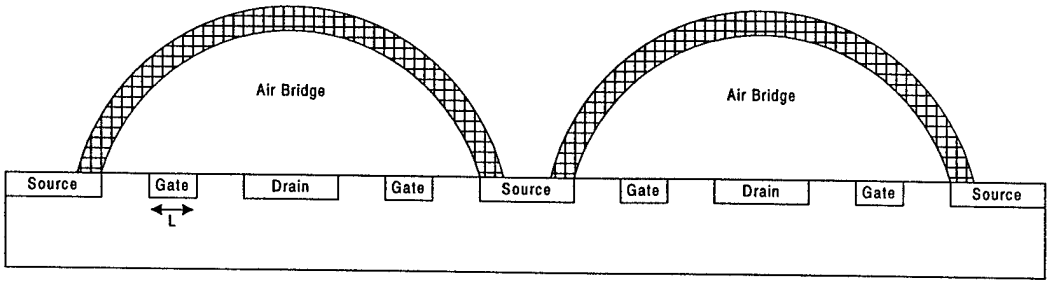


Figure 2. Drawing of Air Bridge Structure (Side View)

throughout the remainder of this discussion. Also shown in Fig. 2 is the gate length, L, which will be referred to later on and is the actual length of the region directly beneath the gate electrode. The gate width mentioned later refers to the total dimension of the gate electrode going into the paper in Fig. 2 and seen vertically in Fig. 1.

After processing and initial on wafer testing, the devices are diced apart, putting each device on a separate physical piece of the wafer. Later in this paper when we discuss multiple devices connected in various tandem arrangements, we will be speaking of connecting devices which lie on different substrate pieces together in series or parallel arrangements. These connections are made by placing the individual device pieces on a common carrier, and then attaching them together using transmission line technology.

Finally, we will discuss at various times the concept of a complete amplifier package. This refers to one or more devices packaged on a carrier with matching circuits included at the chip level. Such an amplifier is said to be commercially ready, i.e. it can be connected into a power amplifier application without requiring additional matching circuitry for proper operation.

For the first part of this discussion, we shall cover the investigation into improving the performance of individual devices, comprised of typically eight transistor regions as seen in Fig. 1. This device level investigation involved analyzing the fundamental physics of the devices and working to improve the material quality of the growths. Second, these single devices were packaged onto carriers for high power RF testing. These units initially did not have any wafer level matching circuits, and all tuning was done externally using microwave tuning elements. As discussed later, this arrangement does not optimize the output power, as the large mismatch at the input side greatly reduces the coupling efficiency of the circuit. Thus, a great deal of effort went into designing the matching circuitry and bias filter circuits in order to alleviate this

problem. Additionally, other packaging concerns, such as the backside substrate attachment to the carrier, were investigated. We shall discuss these issues separately.

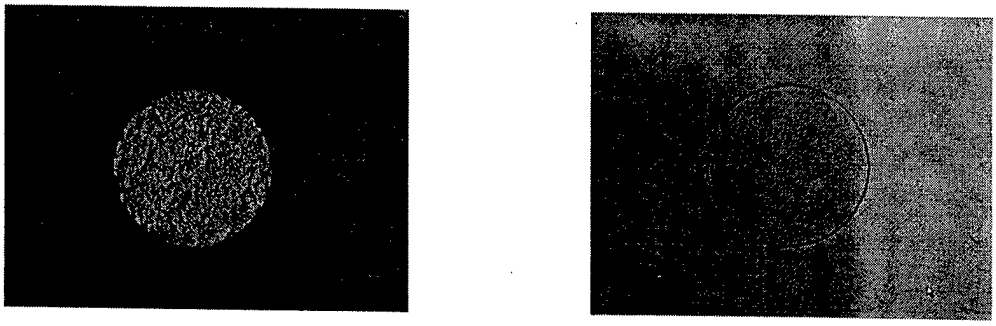
II. Device Work

II-1. Contact Improvement

In order to achieve efficient high power operation for transistor devices, it is essential that the contact resistances at the terminals are as low as possible while at the same time possessing sufficient adhesion and strength properties to last the useful lifetime of the device. Since GaN is a relatively new material system, it was necessary to determine the best contact metalization scheme for both the formation of ohmic contacts and a Schottky barrier for the gate region.

The basic scheme is as follows. First, thin layers of metal are deposited through e-beam metal evaporation. Typically the bottom layer in contact with the semiconductor surface is on the order of 300 Å thick. Successive layers of metal are then deposited again using the e-beam evaporator. Typical thicknesses following the total evaporation sequence are on the order of 3000 Å for ohmic contacts and 7000 Å for gate contacts. After both the source/drain ohmic and the gate Schottky contacts have been deposited, then approximately 2.5 μm of Au is deposited to make contacts suitable for connection to the external circuitry.

For the gate contacts, deposition of Pt followed by Au (Pt/Au) and Pd followed by Au (Pd/Au) were investigated. It was found that both layers formed good Schottky barriers, but the Pt/Au layers did not adhere to the GaN surface as well and some gate peeling was observed during subsequent processing. The Pd/Au samples did not exhibit peel off and had good Schottky barrier characteristics, which principally involve being able to support the gate bias voltage with very low gate leakage current. Subsequent gates were fabricated using the Pd/Au sequence.



(a) (b)

Figure 3. Surface Image of 100 μm diameter mesa structures after annealing with (a) Ti/Al/Pt/Ti/Au and (b) Ta/Au metallization layers

For the ohmic contact formation, more varied layer schemes were investigated. This was due to the more difficult design requirement of forming a very low resistance

connection to the semi-conductor material while maintaining a smooth enough surface to allow good contact formation during the subsequent steps. We tried a number of different metalization recipes for the formation of these ohmic contacts, including: Ti/Al/Pt/Au, Ta/Ti/Al/Ta, Ta/Ti/Al/Pt/ Au, Ti/Au, Ta/Pt/Au, Ti/Al/Pt/Ti/Au, and Ta/Au. It was found that 3000 Å of Ta/Au gave the best overall result.[2] This determination was based on an evaluation of both the overall resistance of the contact and the surface smoothness of the metal following deposition and annealing. It was found that after annealing at high temperatures, several of the materials formed alloys, which degraded the resistive properties of the contact and led to island formation and a rough surface. Fig. 3a shows a 100 μm diameter mesa following annealing. The deposition sequence was Ti/Al/Pt/Ti/Au for a total thickness of approximately 3000 Å. The surface is clearly rough and not suitable for a good contact. Fig. 3b shows a 100 μm diameter mesa following annealing with 2000 Å of Ta/Au deposited. The surface in this case is clearly improved and the contact resistance was less than 1×10^{-6} ohm-cm. It was found that contact resistances of less than 5×10^{-5} ohm-cm did not result in any noticeable degradation in the device current or gain characteristics. This was the contact material that was used in subsequent device processing.

II-2. Gate and Source Air Bridge Design

The next obstacle to overcome in developing a device suitable for high power at the frequencies of interest was to reduce the gate length for higher frequency and higher gain characteristics. It is well known in HFET studies that the unity gain cutoff

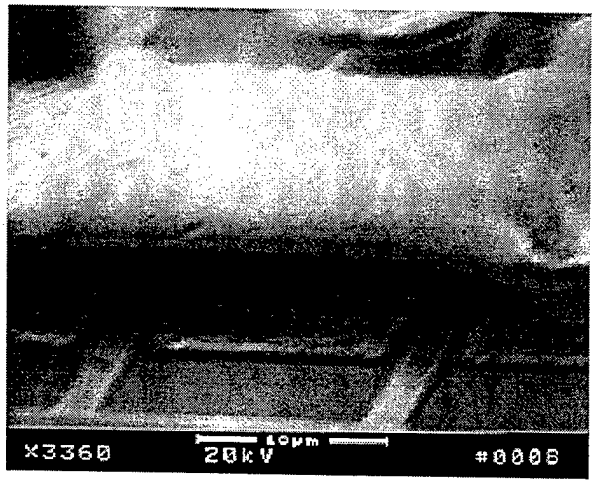


Figure 4. SEM Image of Air Bridge Structure

frequency, f_t, is inversely proportional to the gate length. In our work, our objective was to reduce the gate length using the most cost effective technique, so we developed a new *gamma* gate process. The fabrication of the *gamma* gate design involves both angular deposition and the use of an undercut region, which is formed using standard

photolithography techniques. As a result of reducing the gate length, f_t was improved from 25 GHz to 50 GHz.

In addition, we utilized an air bridge design to allow for three terminal contacts to what is essentially a two dimensional region. Fig. 4 is an scanning electron microscope image of the air bridge structure over the dual gate/drain regions which were mentioned earlier. Again, the air bridges are required when combining multiple active regions in parallel, and serve to connect all of the source regions together without shorting them to either the gate or drain regions. The fabrication of these bridges is not a trivial exercise and required an intense research and development effort to make the process repeatable and uniform.[3]

II-3. Device Compositional Design

During this feasibility study, a concerted effort was also undertaken to optimize the structure of the device as grown by the contracted vendor. Fig. 5 illustrates the basic HFET structure. The doped $Al_xGa_{1-x}N$ layer provides the carriers for device conduction. The carriers are able to make it to the lower energy GaN channel through the thin undoped $Al_xGa_{1-x}N$ layer in a manner analagous to GaAs/AlGaAs HEMT structures. The structure was investigated from a number of design criteria. Essentially, good device characteristics include high sheet carrier, or in this case electron, concentration, high mobility, high saturation current, and high breakdown voltage.

Undoped Cap Layer ($Al_xGa_{(1-x)}N$)
Doped Layer ($Al_xGa_{(1-x)}N$)
Undoped Spacer Layer ($Al_xGa_{(1-x)}N$)
Channel Layer (GaN)
Buffer Layer (GaN)
Sub-Buffer Layer (AlN)
Substrate (SiC or Sapphire)

Figure 5. Basic Composition of HFET Structure.

The first parameter which was varied was the Aluminum (Al) composition of the $Al_xGa_{(1-x)}N$ layers. It was found that the higher the Al composition, the better the sheet concentration and mobility would be for a given doping level. The vendor responsible for the material growth reported however, that Al compositions greater than about 0.4 (40%) resulted in poor growth quality and even in severe cases, sample cracking. The best overall results, which are reported later in this report, were for a sample with a nominal Al concentration of 40%. Post growth analysis, however, shows that the actual composition is closer to 33%.

The doping level within the $Al_xGa_{(1-x)}N$ layer was also varied. The doping levels were pushed as high as possible under the constraint of maintaining crystal quality in

order to raise the sheet concentration to as high a value as possible. Doping levels of 5 x $10^{18}/cm^3$ to 1 x $10^{19}/cm^3$ were typical values for this study.

The breakdown voltage was also a chief concern throughout this study. The higher the breakdown voltage, the higher power the device can, in general, produce since higher breakdown voltages allow for higher voltage swings at the input. We investigated a number of schemes to raise the breakdown voltage including the addition of an undoped cap layer to move the surface away from the region with the highest field intensity. We found that the addition of the cap layer raised the breakdown voltage on the average by a factor of 2. The cap layer, however, may have some detrimental surface effects which reduce the saturation current and limit the overall power capability. The overall effect of the this cap layer is still under investigation.

Finally, in concert with the growth vendor, we investigated the use of a thin AlN buffer layer beneath the GaN buffer layer. The addition of this layer seems to have improved the overall crystal quality and serves to further isolate the substrate from the active region. The utility of this buffer layer is also still being researched.

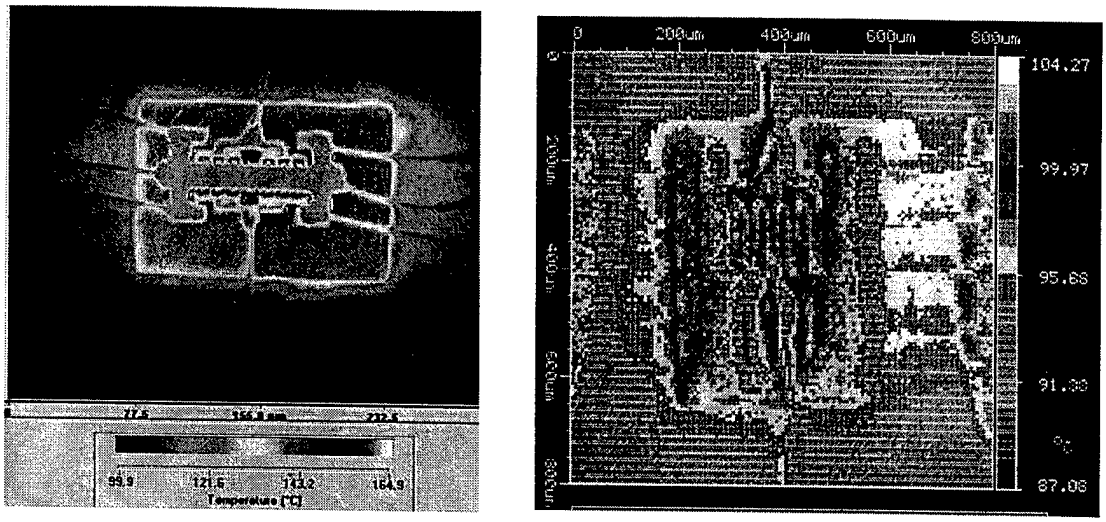
III. Packaging and RF Measurements

In parallel with the efforts to optimize the basic structure of the device through proper selection of doping levels, Al content, spacer layer thickness, and cap layer thickness, a major effort was done on matching circuit design and packaging study. Conjugate matching for both input and output circuits must be carried out in order to achieve the single device (eight active regions) design power level of 5 W. Investigations were also conducted as to the proper method of packaging the devices into an integrated package, taking into account power dissipation and suitability for commercial use. The following paragraphs describe these studies.

III-1. Thermal Management/Packaging

The mobility of GaN material degrades significantly with increasing temperature.[4-5] Although the wide bandgap of the material makes it suitable for operation at junction temperatures in the range of 200-300 C, the reduction in mobility with rising temperature reduces its power handling ability if the temperature is maintained within this range. Since an average power device operates with 20-30% power added efficiency (PAE) in class A-B,[6-7] in order to get 5 W out of such a device (again meaning a single wafer region with eight active areas in parallel), the heat sink must be able to dissipate 20-40 W of DC power without the device temperature rising excessively. We found that our initial device mountings had moderately high thermal resistance, causing a temperature increase of 28 °C per watt as shown in Fig. 6a. Clearly this was insufficient for our purposes. We investigated different materials to use to bond the SiC substrate and device to the amplifier carrier. Both Ni/Cr/Au and Ti/Au were investigated as possible backside metals, with Ti/Au determined to be the best choice. The thickness of all schemes investigated was on the order of 2000 Å. The use of the backside metal improved the "sticking" of the device to the carrier and also served to reduce the thermal resistance. In addition, the die attachment procedure was modified to include the use of an inert atmosphere to minimize the oxidation of the metals being used. It was found that

the use of the gas significantly improved the thermal characteristics of our devices. Both Au/Sn and Au/Ge were investigated as die attachment metals. Both systems are noted for



(a) (b)

Figure 6. IR scans of GaN HFETs. (a) Initial Trial Mounting. R_{th}=28 C°/W. (b) Improved Mounting. R_{th}=9 C°/W

their high melting temperature and low thermal resistance. Fig. 6b shows an IR scan of a GaN HFET using Ti/Au backside metallization. The thermal resistance has been reduced to only 9 degrees per watt. At this value, a device dissipating 25 W of DC power would have a 225 degree temperature rise. At this temperature, the mobility of the GaN channel is projected to be on the order of 500 cm^2/V-sec based on studies from 10 to 300 °K. We have also investigated the possibility of using an on-chip temperature sensor. The temperature dependence of the I-V characteristics of a Schottky diode can, in principle, be exploited to measure the in-channel actual temperature. A design is under way to electrically isolate one of the gate fingers to be used in this manner. By having one of the center gate fingers isolated and connected separately to a sensing circuit, the I-V characteristics of the junction beneath this finger can be monitored and the actual temperature of the in-channel region extracted. Depending upon the results of upcoming temperature experiments, this design may be incorporated into our next mask design.

III-2. Matching Circuits

One of the critical steps in achieving useful output power is to have proper conjugate matching networks at the input and output stages. For testing purposes, external tuners can be used to provide bias matching to the input and output circuits, but this allows for large standing waves to exist within the tuner boundaries due to mismatches at the circuit level. These standing waves and circuit instabilities rob useful output power. A concerted effort is currently underway to provide matching elements

both externally within the bias circuits and at the circuit level on the input and output sides to improve the coupling efficiency and thereby improve the fundamental output power.

Input matching circuits have been designed and tested for improving the transmission of the input signal into the device. Depending on the exact geometry of the gate structure, the input impedance of the HFET device can vary anywhere from 5 to 100 ohms at the frequency of interest. Different matching schemes have been investigated in order to provide optimum input signal matching. The essential element of this procedure

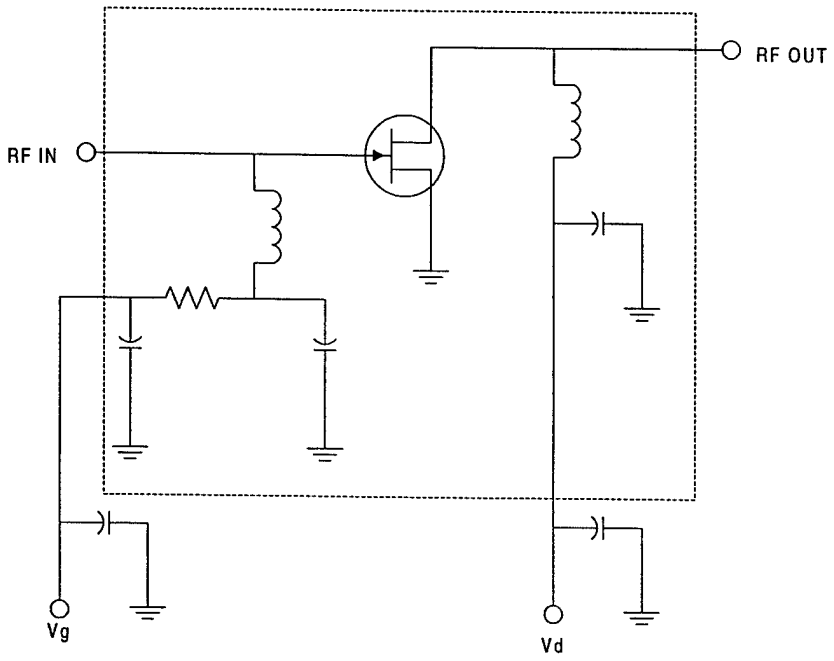


Figure 7. Bias and Matching Circuit for GaN HFET Assembly.

is to place the matching circuit elements as close to the gate as possible. Through proper design of the matching circuitry, the input impedance can be increased, allowing for improved coupling of the signal into the active region of the device. Likewise, the output must be conjugate-matched to achieve maximum output power and high PAE. In our feasibility study, we have demonstrated that proper matching can be done. We are continuing our efforts in this area and the on-chip matching circuits are approaching optimum. Fig. 7 shows an overall schematic of the current amplifier design. The elements within the dotted line are located at the device level, while elements outside of the dotted line are part of the external bias circuitry.

III-3. Power Amplifiers with Combiner Circuits

Along with the circuit matching for individual devices, we have investigated the requirements of matching parallel combined devices. In order to attain the overall project design power level of 20 W, it will be necessary to put four devices in parallel. Figure 8

shows a picture of an amplifier package consisting of four individual devices (each with eight active regions) placed in parallel, alongside a penny for size comparison. Figure 9

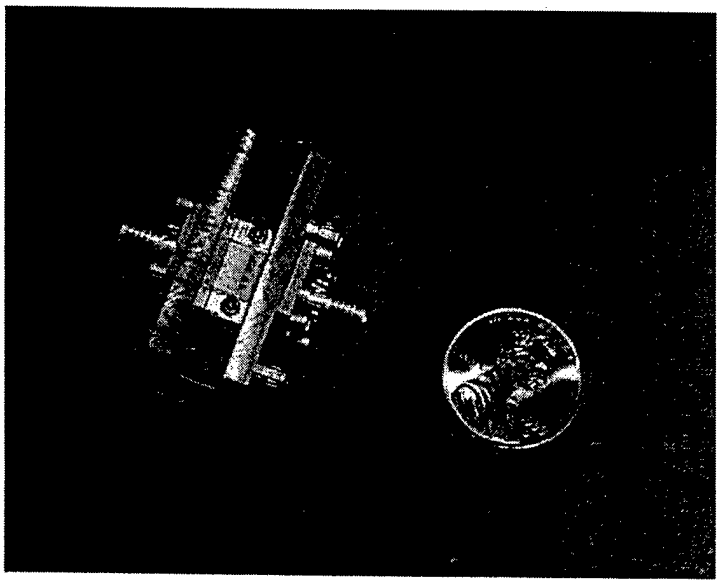


Figure 8. Power Combiner Circuit with 4 HFET Devices

shows a simplified DC schematic with the very general arrangement. This combiner package utilized individual devices with 1 μm x 1.2 mm gate areas. The composite package was tested at various frequencies up to and including 10.0 GHz. Due to

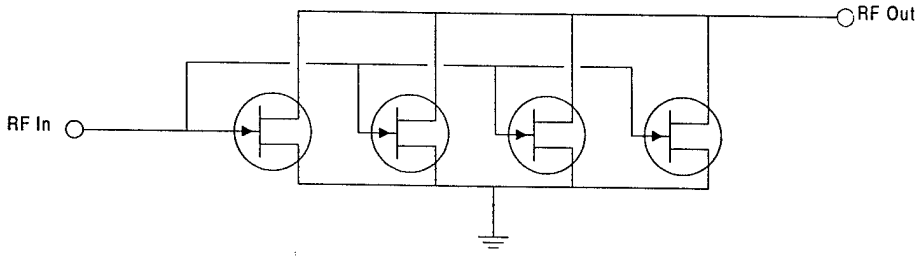


Figure 9. Generalized DC Schematic of Power Combiner Circuit.

deviations from the design values in the matching network, the optimum performance was actually observed at 9.4 GHz and is shown in Figure 10. The output power at this frequency was about 6.0 W with approximately 1 W input power, giving a gain of 4.7 dB

and a PAE of 30.7%. As seen in Fig. 10, gain compression and flattening of P_{out} is minimal, and even higher power levels should be easily obtainable. The results were limited by the current and voltage limitations of the biasing circuit tees, which began to appear at input power levels greater than 33 dBm (2 W). Bias tees with higher power ratings are being acquired for testing at higher powers, and new biasing circuits which are not commercially available are being designed and constructed as discussed earlier. It should be noted that these results were obtained with relatively long gates (1 μm), and we anticipate that this same wafer will produce even better results with shorter gate lengths.

V. Summary

The purpose of this phase I SBIR has been to investigate the feasibility of utilizing GaN based HFETs for high power microwave amplifier applications. Specifically, we investigated whether or not the design objective of 5 W output power

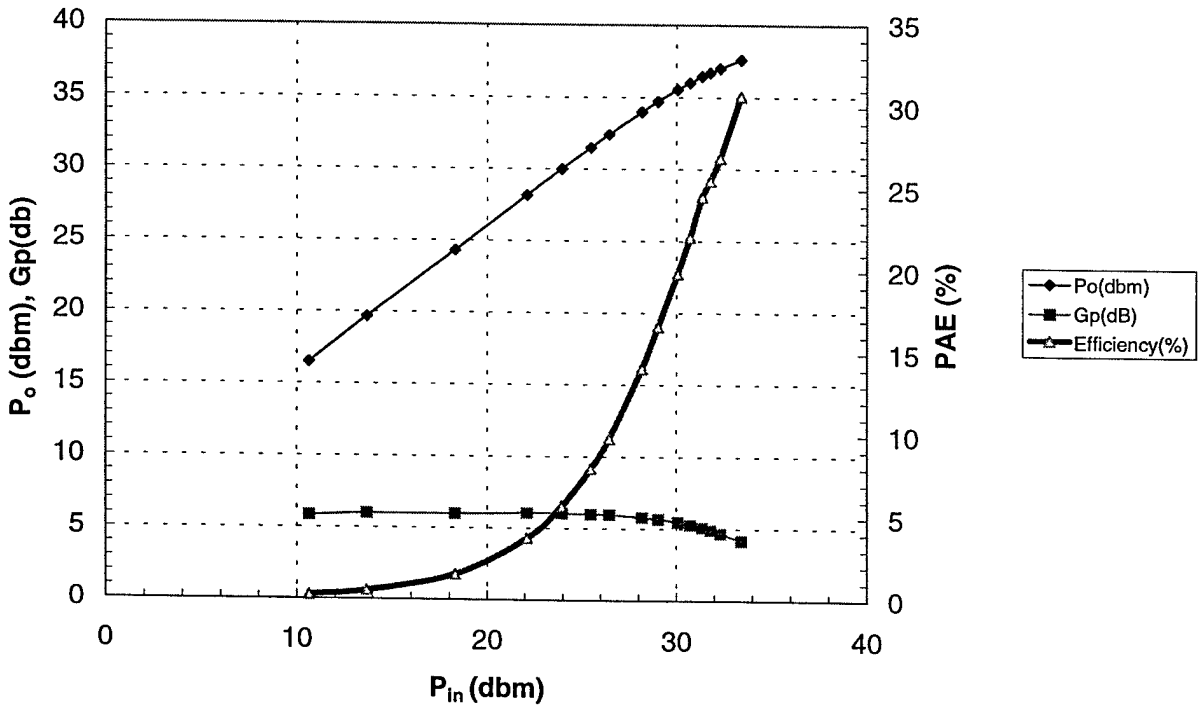


Figure 10. P_{out}, Gain, and PAE vs. P_{in} for 4 Combined HFETs at 9.4 Ghz.

from a single device (comprised of multiple active regions) could be achieved so that the overall objective of 20 W power may be obtained through power combination. Thus far, we have demonstrated 2 W output power at 10 GHz from a single device as well as

nearly 6 W output power from a power combined 4 device amplifier. These results were both achieved using devices with the same gate structure consisting of a 1.0 x 1200 μm total gate electrode size. A power level of greater than 8 W using the present combined power amplifier design should be readily obtained with improved bias circuits. In addition, since the unity gain cutoff frequency, f_t, can be reasonably assumed to be inversely proportional to the gate length, if the gate length is reduced to 0.25 μm, then f_t will increase by a factor approaching 4. Furthermore, the use of 2000 μm periphery devices in contrast with the present 1200 μm devices will have similar gain characteristics but with power levels increasing to 4 ~ 5 W per single device using the existing gate length. We anticipate that these processing improvements will be made in the near future. With further improvements in the carrier attachment design and the on-chip matching circuits, we do not anticipate a problem with heat dissipation at the chip level, but work remains on the package level heat dissipation issue. We have begun investigating several concepts for removing packaged amplifier heat, varying from air to liquid cooling, and we shall investigate these during the Phase II research. With these anticipated improvements, the gain will be increased even more dramatically as the device operating temperature is reduced. When single devices with multiple active regions can be operated at 5-8 W, then power amplifiers consisting of four devices in a power combined configuration and producing 20 W output power should be readily attainable. Thus, it can be seen that the Phase II power objectives of 20 – 100 W output in X-band operation should be attainable without requiring a quantum leap in either technology or device design.

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